d. a second titanium layer directly on the first copper layer; and

e. a second copper layer directly on the second titanium layer.

3. A chip device comprising a wafer, the wafer comprising:

a. a non-passivated wafer;

b. a first substantially pure titanium layer;

c. a first copper layer directly on the first titanium layer;

d. a second titanium layer directly on the first copper layer; and

e. a second copper layer directly on the second titanium layer.

Please cancel claims 4 and 5.

REMARKS

Claims 1-3 are pending.

Claims 1 and 3 stands rejected under 35 USC §102(b) as being anticipated by Mizuhara et al. (U.S. Patent No. 5,898,221).

Claims 1 and 3 stands rejected under 35 USC §102(b) as being anticipated by Bhattacharya (U.S. Patent No. 4,514,751).

Claim 2 stands rejected under 35 USC §103(a) as being unpatentable over Mizuhara et al.

Claim 2 stands rejected under 35 USC §103(a) as being unpatentable over Bhattacharya.

These rejections are respectfully traversed and reconsideration is respectfully requested.

With regard to the rejection of the claims in view of Mizuhara et al., it is respectfully submitted that the reference does not disclose a wafer or a chip device that includes such a wafer, wherein the wafer comprises a first substantially pure titanium layer, a first copper layer directly on the first titanium layer, a second titanium layer directly on the first copper layer, and a second copper layer directly on the second titanium layer as is clearly recited in amended claims 1 and 3. Furthermore, it is respectfully submitted that the titanium layers are actually titanium composites, as opposed to a substantially pure titanium layer as is clearly recited in claims 1 and 3.